

Serial No. 10/783,499

Docket No. Zipfel 1

## SPECIFICATION

## Amend the specification as indicated below:

[0045] In particular, signal PWM is applied to gate driver 33 of amplifier 30. The latter controls a half-bridge comprising FETs 35 and 47 via its output leads 33a and 33b. In particular, when signal PWM is high, lead 33a is (approximately) 10 volts positive with respect to lead 33b, causing FET 35 to be ON and FET 47 to be OFF. A current path is thus established ~~from~~ comprising power supply 31 (supplying a voltage  $V_2$ ), ~~through~~ FET 35, inductor 39, common-mode inductor 41, load L1 and ~~into~~ power supply 32 (supplying a voltage  $V_1$ ), whereby ~~and~~ current  $i_{L1}(t)$  flows through load L1. Conversely, when signal PWM is low, the signals on leads 33a and 33b are reversed, causing FET 35 to be OFF and FET 47 to be ON. A current path is thus established ~~from~~ comprising power supply 32 ~~through~~, load L1, common-mode inductor 41, inductor 39, ~~and~~ FET 47 ~~to and~~ ground, again causing current  $i_{L1}(t)$  to flow through load L1, ~~in the opposite sense~~. Virtually all of the e.m.f. for that current is supplied from energy that was stored in common-mode inductor 41, load L2 and power supply  $V_2$  when signal PWM was high, rather than from power supply 32, as described in further detail below.